What is claimed is:

1. A phase offset calculation method for giving signed binary data a phase offset θ (θ = 90x+y: x=0, ±1, ±2, ±3, ±4, 0<y<90) comprising the steps of:

inverting the sign of said signed binary data to give a phase offset of a multiple of 90°; and

carrying out a phase shift calculation to give the sign-inverted data bit a phase offset with a rotation angle smaller than 90°.

2. The phase offset calculation method according to claim 1, wherein when not only the phase of a signal but also the amplitude is adjusted, the sign of said signed binary data is inverted before the amplitude of the signal is adjusted.

3. A phase offset circuit for giving signed binary data a phase offset θ (θ = 90x+y: x=0, ±1, ±2, ±3, ±4, 0<y<90) comprising:

a sign inversion circuit that gives a phase offset of a multiple of 90° by inverting the sign of said signed binary data; and

a phase shift calculation circuit that gives the data output from said sign inversion circuit a phase offset smaller than 90°.

4. The phase offset circuit according to claim 3, wherein

said phase shift calculation circuit comprises a fixed phase shift calculation section that gives an input signal a predetermined amount of a fixed phase offset, and

whether to output a signal with a fixed phase offset provided by said fixed phase offset section or a signal without said fixed phase offset is selected according to a control signal.

5. A phase offset circuit for giving signed binary data a phase offset θ ($\theta = 90x+y$: x=0, ±1, ±2, ±3, ±4, 0<y<90) comprising:

a sign inversion circuit that gives a phase offset of a multiple of 90° by inverting the sign of said signed binary data;

an amplitude adjustment circuit that adjusts the amplitude of the signal output from said sign inversion circuit; and

a phase shift calculation circuit that gives the signal output from said amplitude adjustment circuit a phase offset smaller than 90°.

6. The phase offset circuit according to claim 5, wherein said phase shift circuit comprises a fixed phase offset section that gives a predetermined amount of a fixed phase offset, and

whether to output a signal with said fixed phase offset provided by said phase offset section or a signal without said fixed phase offset is selected according

to a control signal.

7. A CDMA communication base station apparatus capable of controlling the phase and amplitude of a transmission signal through closed-loop control, comprising:

a phase offset circuit equipped with a sign inversion circuit that gives a phase offset of a multiple of 90° by inverting the sign of a QPSK modulated signal, an amplitude adjustment circuit that adjusts the amplitude of the signal output from said sign inversion circuit and a phase offset circuit that gives the signal output from said amplitude adjustment circuit a phase offset smaller than 90°; and

a transmission control section that provides phase control information to said phase offset circuit based on a message from a mobile station included in a reception signal.

8. The CDMA communication base station apparatus according to claim 7, wherein said phase offset circuit further comprises a fixed phase offset section that gives a predetermined amount of a fixed phase offset, and

whether to output a signal with a fixed phase offset provided or a signal without said fixed phase offset is selected according to said phase control information given by said transmission control means.

9. The CDMA communication base station apparatus

according to claim 7, wherein control of the phase and amplitude can be performed for every transmit channel.

10. A closed-loop mode transmit diversity method that controls the phase and amplitude of a signal transmitted from an antenna based on a message from the other end of communication, comprising the steps of:

giving a phase offset of a multiple of 90° by inverting the sign of a QPSK modulated signal;

adjusting the amplitude of the signal subjected to said sign inversion processing; and

giving a phase offset smaller than 90° to the signal subjected to said amplitude adjustment processing.

11. A phase offset circuit that gives a QPSK modulated signal a phase offset, comprising:

a sign inversion circuit that gives a phase offset of a multiple of 90° by inverting the sign of the QPSK modulated signal;

an amplitude adjustment circuit that adjusts the amplitude of the signal output from said sign inversion circuit; and

a phase shift calculation circuit that gives a phase offset smaller than 90° to the signal output from said amplitude adjustment circuit.

12. The phase offset circuit according to claim 11, wherein the phase offset circuit can give an input signal 8 types

of phase offset of +180°, -135°, -90°, -45°, 0°, +45°, +90° and +135°.